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According to the Applicant's claimed invention, thermal stresses generated from the heat sink can be released via the **hollow parts** formed in the heat sink, such that delamination of the heat sink from the chip or semiconductor package can be prevented (see specification at page 10, line 21 to page 11, line 4). Also, problems such as chip cracking, structural warpage, and deterioration of electrical connections can be eliminated using the Applicant's claimed invention (see, e.g., specification at page 12, lines 3-8).

Claims 1-4 and 6-8 were rejected under 35 USC 102(a) as being anticipated by "Admitted Prior Art (APA), figures 1-3." Claim 5 was rejected under 35 USC 103(a) as being unpatentable over "APA" in view of U.S. Patent 5,598,033 to Behlen et al. These rejections are respectfully traversed.

APA does not teach or suggest a multi-chip package with a heat sink including at least one hollow part extending through the heat sink that is formed at an area of the heat sink free of contact with a first chip and a semiconductor package (see claim 1).

In the Office Action of 05/17/2006, it was alleged that "APA" discloses the Applicant's claimed multi-chip package including "at least one hollow part extending through the heat sink" that is formed at an area of the heat sink free of contact with a first chip and a semiconductor package (see Office Action at page 2, last four lines; and "attachment" referencing PRIOR ART FIG. 2 of the application).

Referring to PRIOR ART FIG. 2, the multi-chip package device of "APA" includes a chip carrier 20, at least one first chip 21 mounted on and electrically connected to a surface of the chip carrier 20, at least one semiconductor package 22, and a heat sink 24 mounted via an adhesion layer 23 on a surface of the first chip 21 and a surface of the semiconductor package 22.

In PRIOR ART FIG. 2, an area identified in the Office Action as allegedly corresponding to the claimed "hollow part" is enclosed by the chip carrier 20, the first chip 21, the semiconductor package 22, the adhesion layer 23, and the heat sink 24.

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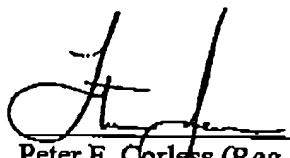
Therefore, the "hollow part" of PRIOR ART FIG. 2 does not extend through the heat sink as claimed, but instead is located outside the heat sink 24. Also, the "hollow part" of PRIOR ART FIG. 2 is not "free of contact with the first chip and the semiconductor package" as claimed. In PRIOR ART FIG. 2, the "hollow part" is formed adjacent the first chip 21 and the semiconductor package 22.

Moreover, the "APA" suffers from significant problems such as mismatch in coefficient of thermal expansion (CTE) among the chip carrier 20, the first chip 21, the semiconductor package 22, the adhesion layer 23, and the heat sink 24 when the package assembly is subject to subsequent fabrication processes, which can produce thermal stresses that may degrade package quality (see specification at page 3, lines 17-24).

For at least the reasons discussed above, "APA" does not anticipate or otherwise render obvious the Applicant's claimed invention. Therefore, independent claim 1 and dependent claims 2-8 are patentable over "APA."

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,



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